



UTT70N06

Preliminary

Power MOSFET

70 Amps, 60 Volts N-CHANNEL POWER MOSFET

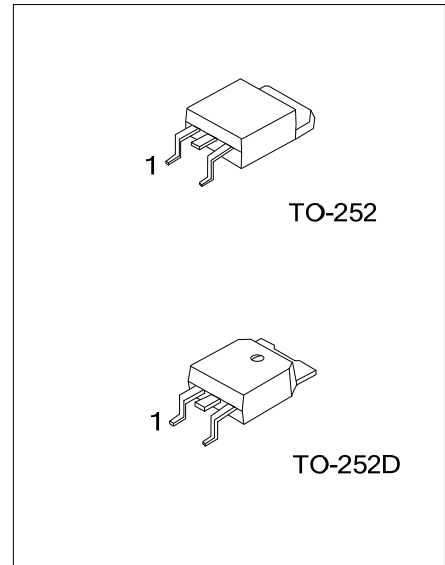
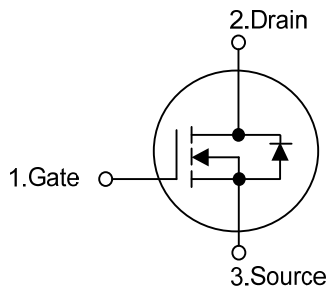
DESCRIPTION

The UTC **UTT70N06** is n-channel enhancement mode power field effect transistors with stable off-state characteristics, fast switching speed, low thermal resistance, usually used at telecom and computer application.

FEATURES

- * $R_{DS(ON)} < 10 \text{ m}\Omega @ V_{GS} = 10 \text{ V}, I_D = 35 \text{ A}$
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability

SYMBOL



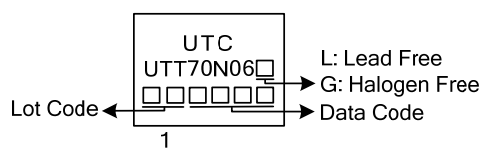
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT70N06L-TN3-R	UTT70N06G-TN3-R	TO-252	G	D	S	Tape Reel
UTT70N06L-TND-R	UTT70N06G-TND-R	TO-252D	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT70N06L-TN3-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252, TND: TO-252D (3) L: Lead Free, G: Halogen Free and Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	A
Drain Current Pulsed (Note 2)	I_{DM}	280	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	10	V/ns
Power Dissipation	P_D	50	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repeativity rating: pulse width limited by junction temperature

3. $L=0.1\text{mH}$, $I_{AS}=40\text{A}$, $V_{DD}=25\text{V}$, $R_G=20\Omega$, Starting $T_J=25^\circ\text{C}$

4. $I_{SD}\leq 48\text{A}$, $di/dt\leq 300\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

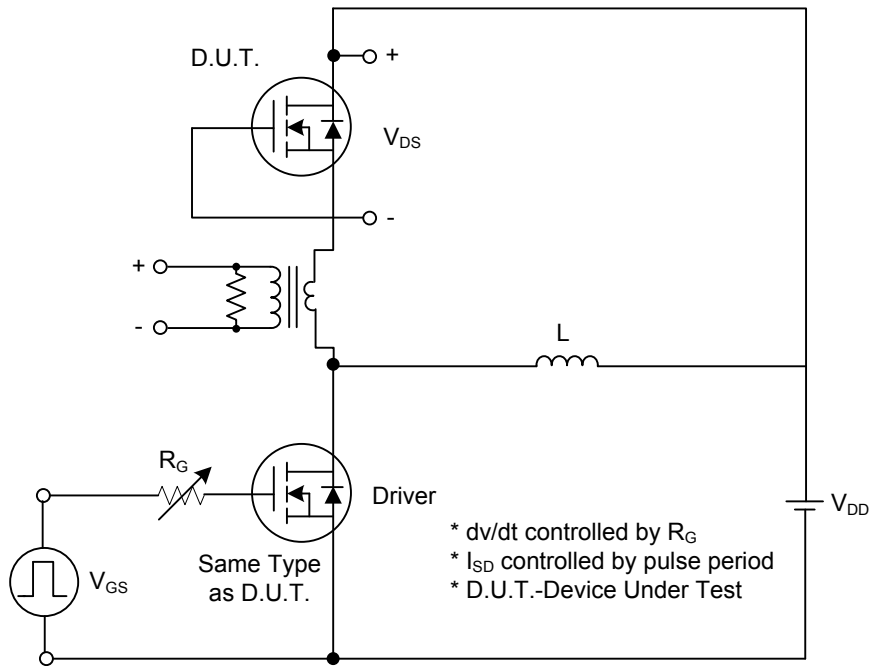
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.5	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_c = 25°C, unless otherwise specified)

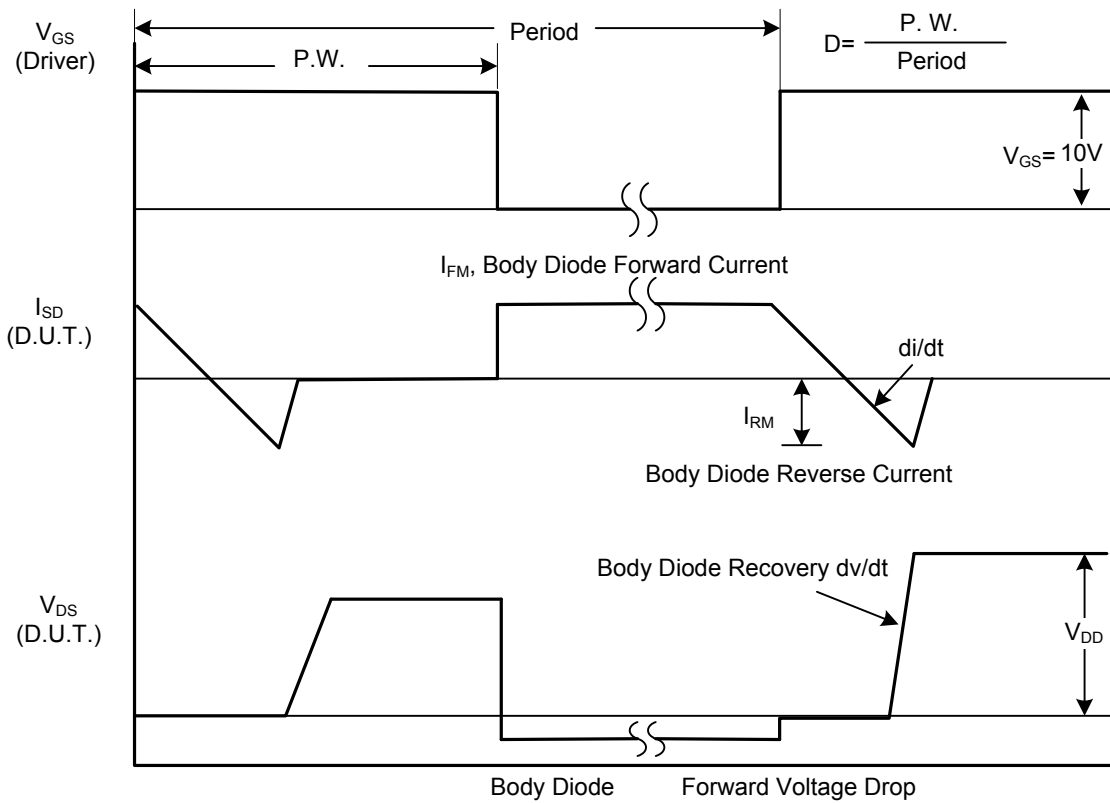
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS} V _{GS} =20V, V _{DS} =0V V _{GS} =-20V, V _{DS} =0V			100	nA
	Reverse				-100	nA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D = 1mA, Referenced to 25°C		0.08		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =35A			10	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1MHz		3500		pF
Output Capacitance	C _{OSS}			310		pF
Reverse Transfer Capacitance	C _{RSS}			55		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V, V _{GS} =10V, I _D =0.5A (Note 1, 2)		125		ns
Turn-On Rise Time	t _R			160		ns
Turn-Off Delay Time	t _{D(OFF)}			720		ns
Turn-Off Fall Time	t _F			200		ns
Total Gate Charge	Q _G	V _{DS} =50V, V _{GS} =10V, I _D =48A, I _G =100μA (Note 1, 2)		275		nC
Gate-Source Charge	Q _{GS}			18		nC
Gate-Drain Charge (Miller Charge)	Q _{GD}			41		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =70A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I _S				70	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				280	
Reverse Recovery Time	t _{RR}	V _{GS} =0V, I _S =70A dI _F /dt=100A/μs		90		ns
Reverse Recovery Charge	Q _{RR}			300		μC

Notes: 1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
 2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



1A Peak Diode Recovery dv/dt Test Circuit



1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

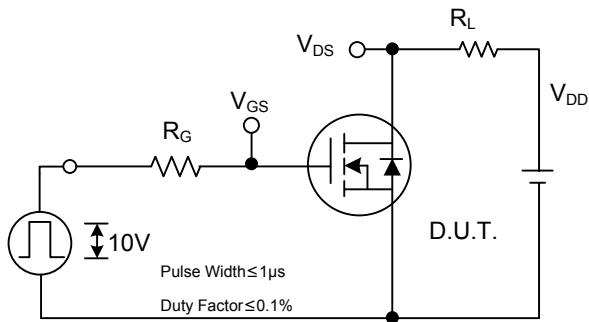


Fig. 2A Switching Test Circuit

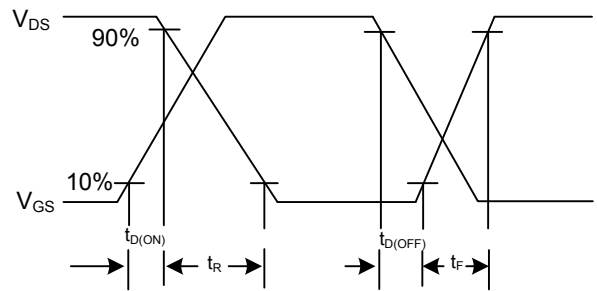


Fig. 2B Switching Waveforms

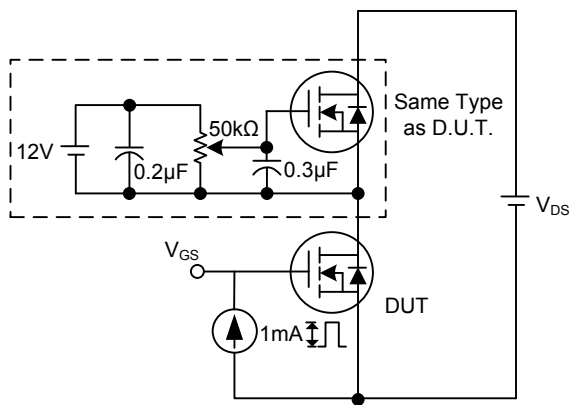


Fig. 3A Gate Charge Test Circuit

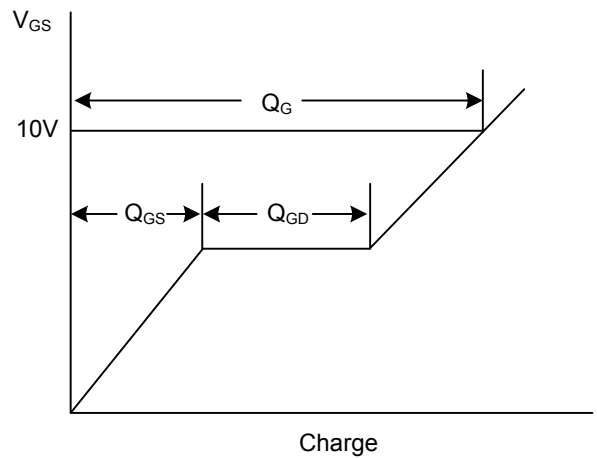


Fig. 3B Gate Charge Waveform

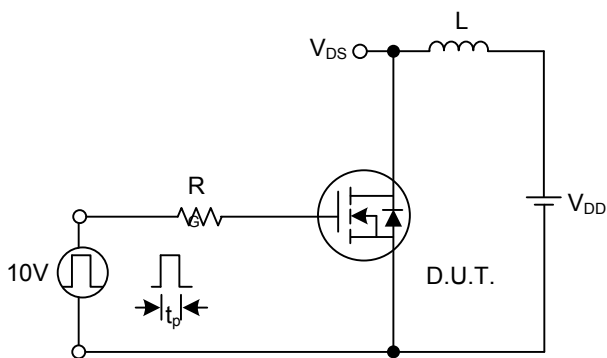


Fig. 4A Unclamped Inductive Switching Test Circuit

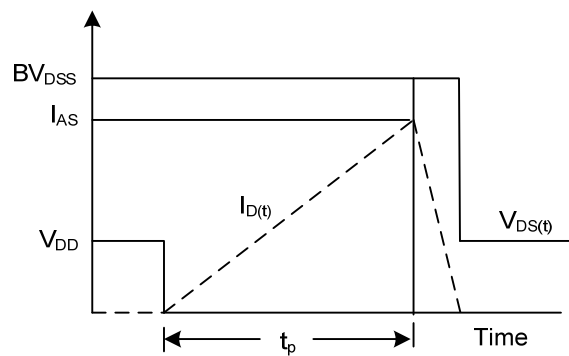


Fig. 4B Unclamped Inductive Switching Waveforms

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